

Customer No.: 31561
Docket No.: 12792-US-PA
Application No.: 10/709,488

AMENDMENT

Please amend the application as indicated hereafter.

To the Claims:

Claim 1 (Currently Amended) A circuit for performing pulse width modulation suitable for generating a PWM signal according to an input data with $M+N$ bits, the pulse width of the PWM signal dithering in 2^N frames and corresponding to a value of the input data, comprising:

a pulse density modulator (PDM), for receiving the least N bits of the input data and generating a pulse density modulation signal, wherein a number of pulse of the pulse density modulation signal in 2^N frames correspond to a value of the least N bits of the input data;

a first adder, electrically coupled to the PDM for generating a PWM data by adding the most M bits of the input data to a value of the pulse density modulation signal; and

a pulse width modulator, electrically coupled to the first adder for generating a PWM signal dithering in 2^N frames according to the PWM data,

wherein the PWM signal comprises a positive PWM signal and a negative PWM signal.

Claim 2 (Original) The circuit for performing pulse width modulation of claim 1, wherein the PDM comprises:

a latch; and

a second adder, electrically coupled to the latch for generating a carry and a summation by adding a value of the least N bits of the input data to an output of the latch,

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outputting the carry as the pulse density modulation signal, and updating the latch with the summation when converting the frame.

Claim 3 (Original) The circuit of performing pulse width modulation of claim 1, wherein before a value of the most M bits of the input data is added to the value of the pulse density modulation signal by the first adder, the M bits input data is sign-extended to an input data with at least M+1 bits, so as to generate a PWM data with at least M+1 bits.

Claim 4 (Currently Amended) The circuit of performing pulse width modulation of claim 3, wherein ~~the PWM signal comprises a positive PWM signal and a negative PWM signal, and the pulse width modulator comprises:~~

a latch, electrically coupled to the first adder for updating the latch value with the PWM data when converting the frame;

an absolute value calculator, electrically coupled to the latch for generating an absolute value of the PWM data output from the latch;

a counter, for generating a counting value according to an operating clock;

a comparator, electrically coupled to the counter and the absolute value calculator for generating a comparison signal by comparing the absolute value of the PWM data with the counting value; and

a PWM output switch, electrically coupled to the latch and the comparator for switching the comparison signal to either the positive PWM signal or the negative PWM signal according to a signed bit of the PWM data output from the latch.

Claim 5 (Original) The circuit for performing pulse width modulation of claim 4, wherein the absolute value calculator is made of an XOR gate.

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Claim 6 (Currently Amended) A method of performing pulse width modulation suitable for generating a PWM signal according to an input data with $M+N$ bits, the pulse width of the PWM signal dithering in 2^N frames and corresponding to a value of the input data, comprising:

receiving least N bits of the input data, and generating a pulse density modulation signal, wherein a number of the pulse of the pulse density modulation signal in 2^N frames correspond to a value of the least N bits of the input data;

generating a PWM data by adding most M bits of the input data to a value of the pulse density modulation signal; and

generating a PWM signal dithering in 2^N frames according to the PWM data,
wherein the PWM signal comprises a positive PWM signal and a negative PWM signal.

Claim 7 (Original) The method of performing pulse width modulation of claim 6, wherein before adding the value of the most M bits of the input data to the value of the pulse density modulation signal, the M bits input data is sign-extended to an input data with at least $M+1$ bits, so as to generate a PWM data with at least $M+1$ bits.

Claim 8 (Currently Amended) The method of performing pulse width modulation of claim 7, ~~wherein the PWM signal comprises a positive PWM signal and a negative PWM signal,~~ and the step of generating ~~a dithering~~ the PWM signal dithering comprises:

calculating an absolute value of the PWM data;

generating a counting value according to an operating clock;

generating a comparison signal by comparing the absolute value of the PWM data with the counting value; and

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switching the comparison signal to either the positive PWM signal or the negative
PWM signal according to a signed bit of the PWM data.